INTELLIGENT TEST VECTOR FORMATTING TO REDUCE TEST VECTOR SIZE AND ALLOW ENCRYPTION THEREOF FOR INTEGRATED CIRCUIT TESTING

ABSTRACT OF THE DISCLOSURE

A method and circuit for testing an integrated circuit device using intelligent test vector formatting that reduces the storage required for test patterns and also provides encryption of the test patterns. A first memory stores a test vector mask that is a sequence of bits to indicate if corresponding test vector data is deterministic or random. The test vector data contains a portion that is deterministically generated by automatic test pattern generation (ATPG) software and a portion that is random. A second memory contains a sequence of bits that represent the deterministic test vector data. A random number generator (e.g., linear feed-back shift register, LFSR) generates a reproducible sequence of pseudo random bits that is based on a seed value. A selector circuit is used to select bits either from the second memory or from the random number generator based on the value of the mask vector. The output of the selector provides a fully specified test vector for application to the device under test (DUT). The LFSR can be fabricated on the DUT. The output of the DUT can be coupled back to stages of the LFSR. The bits of the mask vector can readily be compressed thereby saving memory. Neither the first or second memory need to store the random bits because these bits are reproduced on-the-fly by the LFSR, viewed as a compressed data repository. The system provides encryption protection for the test vectors because the LFSR requires the proper seed value before generating the proper sequence of pseudo random bits.